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METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

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METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method of manufacturing a semiconductor device, and more particularly, to a method of forming a floating gate in a flash memory device by which the floating gate is formed in the self-aligned mode.

Background of the Related Art

Recently, as the design rule is reduced and the size of the device is reduced, it is difficult to control overlapping of a field oxide film (FOX) that has the greatest influence on the distance between the floating gates and coupling in the ETOX (EEPROM tunnel oxide) cell. In general, the flash memory cell is implemented using the STI process. Upon isolation of the floating gate, the uniformity of the wafer depending on variation of the critical dimension (CD) is not easy in the patterning process using the mask. For this reason, there is a problem that the coupling ratio between the devices is not uniform. Furthermore, if a high bias voltage is applied during the programming or erasing operation of the flash memory devices, defective flash memory devices may occur due to a uniform floating gate. In addition, the production yield is degraded and the cost price is increased, due to

misalignment between the isolation mask and the poly mask and an increased mask process.

SUMMARY OF THE INVENTION

Accordingly, the present invention is contrived to substantially obviate one or more problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide a method of manufacturing a semiconductor device capable of forming a floating gate without using the mask process and forming the floating gate of a small size, in such a manner that in a state that a tunnel oxide film and first polysilicon film for forming a floating gate are deposited, a patterning process is implemented to form an isolation film of a STI structure and a second polysilicon film is deposited on the first polysilicon film, thus forming a floating gate.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a method of manufacturing a semiconductor device according to the present

invention is characterized in that it comprises the steps of sequentially forming a tunnel oxide film, a first polysilicon film and a pad nitride film on a semiconductor substrate, etching portions of the pad nitride film, the first polysilicon film, the tunnel oxide film and the semiconductor substrate by means of a patterning process to form a trench within the semiconductor substrate, depositing an oxide film on the entire structure including the trench and then planarization the oxide film so that the pad nitride film is exposed, etching the pad nitride film to form an oxide film protrusion, depositing a second polysilicon film on the entire structure and then planarization the second polysilicon film so that the oxide film protrusion is exposed, and etching a part of the exposed oxide film protrusion to form a floating gate, and then forming a dielectric film and a control gate.

In another aspect of the present invention, it is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will be apparent from the following detailed description of the preferred embodiments of the invention in conjunction with the accompanying drawings, in which:

FIG. 1A ~ FIG. 1G are cross-sectional views of semiconductor devices for explaining a method of manufacturing the device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings, in which like reference numerals are used to identify the same or similar parts.

FIG. 1A ~ FIG. 1G are cross-sectional views of semiconductor devices for explaining a method of manufacturing the device.

Referring now to FIG. 1A, a screen oxide film (not shown), which is necessary for prohibition of crystal defects on the substrate surface or surface treatment and serves as a buffer layer upon implantation of ions, is deposited on a semiconductor substrate **10**. Ion implantation is then implemented to form a well. After the screen oxide film is removed, a tunnel oxide film **12**, a first polysilicon film **14** and a pad nitride film **16** are deposited.

In more concrete, before the screen oxide film is formed, in order to clean the semiconductor substrate **10**, a pre-treatment cleaning process is implemented using DHF (dilute HF) in which H_2O and HF are mixed at the ratio of 50:1 and SC-1 (standard cleaning - 1) consisting of NH_4OH, H_2O_2 and H_2O, or BOE (buffered oxide etchant) in which NH_4F and HF are mixed at the ratio of 100:1 ~ 300:1 and SC-1 consisting of NH_4OH, H_2O_2 and H_2O. Dry or wet oxidization process is implemented at a temperature of 750 ~ 800℃ to form the screen oxide film of 30 ~ 100Å in thickness.

After the ion implantation, the screen oxide film is etched using DHF in which H_2O and HF are mixed at the ratio of 50:1 and SC-1 consisting of

NH_4OH, H_2O_2 and H_2O. Next, the tunnel oxide film **12** is formed in thickness of 85 ~ 110Å by means of a wet oxidization method at a temperature of 750 ~ 800℃. After deposition of the tunnel oxide film **12**, an annealing process is implemented using N_2 at a temperature of 900 ~ 910℃ for 20 ~ 30 minutes. Thereby, the defect density at the interface between the tunnel oxide film **12** and the semiconductor substrate **10** is minimized.

A first polysilicon film **14** having thickness of 200 ~ 1000Å is deposited on the tunnel oxide film **12** using SiH_4 or Si_2H_6 and PH_3 gas by means of a chemical vapor deposition (CVD), a low pressure CVD (LPCVD), a plasma enhanced CVD (PECVD) or an atmospheric pressure CVD (APCVD) method at a temperature of 530 ~ 680℃ under a pressure of 0.1 ~ 3.0torr. Due to this, as the granularity of the first polysilicon film **14** is minimized, it is possible to prevent concentration of an electric field. Next, a pad nitride film **16** having a thickness of about 1300 ~ 3000Å is formed on the first polysilicon film **14** by means of the LP-CVD method.

Referring to FIG. 1B, the pad nitride film **16**, the first polysilicon film **14**, the tunnel oxide film **12** and the semiconductor substrate **10** are sequentially etched through ISO mask patterning, to form a trench **18** of a STI (shallow trench isolation) structure, so that an active region and a field region are defined. A dry oxidization process for compensating for etch damage of the sidewall of the trench **18** of the STI structure is implemented. A rapid thermal process is also implemented to make rounded the corners of the trenches **18**. High temperature oxide (HTO) is thinly deposited on the entire structure and a densification process is implemented at high temperature to

form a liner oxide film (not shown).

In concrete, after a photoresist film is covered on the entire structure, a photolithography process using a photoresist film mask is implemented to form a photoresist film pattern (not shown). An etch process using the photoresist film pattern as an etch mask is then implemented to etch the pad nitride film **16**, the first polysilicon film **14**, the tunnel oxide film **12** and the semiconductor substrate **10**, thus forming the trench **18** of the STI structure. For the purpose of compensating for damage of the sidewall of the trench **18** due to the etch process, a dry oxidization process is implemented within a temperature range of 800 ~ 1000℃, thereby forming a sidewall oxide film of 50 ~ 150Å in thickness.

A rapid thermal process (RTP) using hydrogen is implemented (using a property that atoms of the semiconductor substrate are moved) to make rounded the corner and edged elements of the trench. It is thus possible to prohibit concentration of the electric field and improve the device operating characteristic. At this time, the RTP is implemented by introducing a hydrogen gas of 100 ~ 2000sccm at a temperature of 600 ~ 1050℃ under a pressure of 300 ~ 380torr for 5 ~ 15minutes in a fast thermal process (FTP) type equipment.

In order to improve an adhesive characteristic between the oxide film and the trench **18** in a subsequent process and prevent generation of a moat, HTO formed using DCS (dichloro silane; SiH_2Cl_2) gas is deposited in thickness of 50 ~ 150Å, A high temperature densification process is then implemented using N_2 at a temperature of 1000 ~ 1100℃ for **20** ~ **30** minutes

to form a liner oxide film (not shown). The tissue of the liner oxide film is made dense by the high temperature densification process. Accordingly, an etch resistance is increased, formation of the moat is prohibited upon implementation of STI and the leakage current is prevented.

Referring to FIG. 1C, a high density plasma (HDP) oxide film **20** is deposited on the entire structure to bury the trench **18**. A planarization process using the pad nitride film **16** as a stop layer is then implemented. A planarization process for removing the HDP oxide film **20** and the liner oxide film on the pad nitride film **16** is implemented using the pad nitride film **16** as an etch stop layer.

In more concrete, in order to fill the gap of the trench **18**, the HDP (high density plasma) oxide film **20** is formed in thickness of 5000 ~ 10000 Å. At this time, the HDP oxide film **20** is deposited so that an empty gap is not formed within the trench **18**.

After a planarization process using CMP is implemented, a post cleaning process using BOE or HF is implemented in order to remove the oxide film that may remain on the pad nitride film **16**. At this time, it is strongly recommended that reduction in the height of the HDP oxide film **20** due to over-etch should be prohibited by maximum.

Referring to FIG. 1D, the pad nitride film **16** is experienced by a nitride strip process using H_3PO_4 dip out, thereby forming a HDP oxide film protrusion **22**. When the pad nitride film **16** is tripped, it is required that the height of the HDP oxide film protrusion **22** from the first polysilicon film **14** be about 700 ~ 2500 Å. At this time, it is preferred that the step between the

first polysilicon film **14** and the field oxide film has a thickness used in a second polysilicon film formed in a subsequent process plus a small thickness of about 200 ~ 300 Å.

Referring to FIG. 1E, after a pre-treatment cleaning process is implemented, a second polysilicon film **24** is deposited on the entire structure. A planarization process is then implemented to remove the second polysilicon film **24** formed on the HDP oxide film protrusion **22**, thereby forming a floating gate electrode **26**.

In concrete, a pre-treatment wet cleaning process using DHF and SC-1 is implemented to form an overlapped portion between the field oxide film and the polysilicon film. At this time, it is possible to prevent formation of a moat in the cell region and loss of the tunnel oxide film **12** below the first polysilicon film **14**, by controlling a wet cleaning time. Also, the wet cleaning process may be controlled so that 2/3 of the thickness of the first polysilicon film **14** (100 ~ 700 Å) is opened.

Thereafter, the second polysilicon film **24** having the same material to the first polysilicon film **14** is deposited in thickness of 800 ~ 2500 Å to bury the HDP oxide film protrusion **22**. In order to prevent deviation that may occur in the planarization process using CMP, a buffer layer (not shown) such as PE-TEOS (plasma enhanced tetra ethyle ortho silicate), PE-Nit, PSG (phosphorus silicate glass) and BPSG (boron phosphorus silicate glass) is formed by means of the PE-CVD method. At this time, the buffer layer is deposited in thickness of 100 ~ 1000 Å.

The buffer layer and the second polysilicon film **24** on the HDP oxide

film protrusion **22** are removed by the chemical mechanical polishing (CMP) process and the second polysilicon film **24** is thus isolated. Accordingly, a floating gate electrode **26** consisting of the first and second polysilicon films **14** and **24** is formed. Furthermore, the CMP process is implemented so that the floating gate electrode (total thickness of the first and second polysilicon films) remains uniformly in thickness of 1000 ~ 2500Å.

Referring to FIG. 1f, after the CMP process, the exposed HDP oxide film protrusion **22** is removed in thickness of 500 ~ 2000Å by means of a pre-treatment cleaning process using HF or BOE. This allows the width and surface area of the floating gate electrode **26** to be smaller than when being implemented using the existing masking process, so that the coupling ratio can be high.

By reference to FIG. 1G, a dielectric film **28** is formed along the step of the entire structure. A third polysilicon film **30** and a tungsten silicide (Wsi) film **32** for forming the control gate are then sequentially deposited.

In concrete, the dielectric films of various shapes used in the semiconductor devices may be deposited. In the present embodiment, however, the dielectric film **28** of an ONO (oxide film/nitride film/oxide film (SiO_2-Si_3N_4-SiO_2)) or ONON structure is deposited. In the dielectric film **28** of the ONO structure, the oxide film in the ONO structure is deposited in thickness of about 35 ~ 60Å using DCS (SiH_2Cl_2) and N_2O gas having good withstanding voltage and TDDB characteristic under a low pressure of 0.1 ~ 3torr at a temperature of about 810 ~ 850℃ by means of the LP-CVD method. Also, the nitride film in the ONO structure is deposited in thickness of about

50 ~ 65Å using DCS and NH_3 gas under a low pressure of 1 ~ 3torr at a temperature of about 650 ~ 800℃ by means of the LP-CVD method.

After the ONO process is implemented, in order to improve the quality of the ONO oxide film and enhance the interface between the respective layers, a steam anneal process may be implemented at a temperature of about 750 ~ 800℃ in a set oxidization mode so that the oxide film is oxidized in thickness of about 150 ~ 300Å in case of a monitoring wafer. Furthermore, when the ONO process and the steam anneal process are implemented, they are implemented with no time delay within several hours among the respective processes, so that the ONO oxide film is prevented from being contaminated by a native oxide film or an impurity.

A third polysilicon film **30** has a dual structure of a doped film and an undoped film and is deposited using an amorphous silicon film at a temperature of about 510 ~ 550℃ under a pressure of 1.0 ~ 3torr by means of the LP-CVD method, in order to prevent diffusion of fluoric acid that is substitutively solidified into the dielectric film **28** when the tungsten silicide film **32** is deposited and may increase the thickness of the oxide film. At this time, the ratio of the doped film and the undoped film is 1:2 ~ 6:1, and the amorphous silicon film is formed in thickness of about 500 ~ 1000Å so that the gap between the floating gate electrodes **26** is sufficiently buried. Therefore, when the subsequent tungsten silicide film **24** is deposited, formation of a crack is prohibited and the word line resistance (Rs) could be thus reduced. When the third polysilicon film of the dual structure is formed, it is preferred that the doped film is formed using SiH_4 or Si_2H_6 and PH_3 gas,

PH_3 gas is then blocked and the undoped film is consecutively formed.

It is preferred that the tungsten silicide film **32** is grown in stoichiometry of about 2.0 ~ 2.8, which can implement an adequate step coverage and minimize the word line resistance (Rs), at a temperature of 300 ~ 500℃ using reaction of MS(SiH_4) or DCS(SiH_2CL_2) and WF_6 containing low fluorine and having a low post annealed stress and a good adhesive strength.

An ACR layer (not shown) is deposited on the tungsten silicide film **32** using SiO_xN_y or Si_3N_4. A gate mask and etching process and a self aligned mask and etching process are implemented to form a control gate electrode.

As described above, according to the present invention, the floating gate, which was formed through the existing mask and etch processes, is formed by forming oxide film protrusions on a field oxide film and forming a floating gate between the oxide film protrusions. Therefore, the present invention has advantageous effects that it can minimize the critical dimension of the device, facilitate the size of the device and can form a uniform floating gate over the wafer.

Furthermore, the present invention has new effects that it can improve characteristics of the flash memory devices since the difference of the coupling ratio between the cells is reduced due to the uniform floating gate and can maximize the coupling ratio since the active critical dimension is small.

In addition, the conventional mask process is obviated. Therefore, the present invention has new effects that it can solve problems that may occur in the masking process, simplify the process, improve the yield and reduce the cost price.

Incidentally, the present invention has an advantageous effect that it can easily secure various process margins by controlling the height and distance of the oxide film protrusion.

The forgoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The present teachings can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.